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A 200 MHz AUTORANGING MECL–McMOS FREQUENCY COUNTER

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The principles of an autoranging counter are discussed and a design for a 200 MHz MECL – McMOS counter is also presented.

MOTOROLA *Semiconductor Products Inc.*

A 200 MHz AUTORANGING MECL-McMOS FREQUENCY COUNTER

INTRODUCTION

The increasing variety and complexity of integrated circuits has made possible more sophisticated electronics equipment than ever before. At the same time, the equipment is smaller in size, and often much easier to use. Digital test gear for instrumentation is a good example of this fact.

Digital test meters such as DVM's, multimeters, and frequency counters are becoming more automatic and often offer greater resolution, higher frequency, or similar higher performance. The following discussion is of such an instrument – a 200 MHz autoranging frequency counter. The principles of an autoranging counter are first discussed, and then a MECL – McMOS design is described.

BASIC COUNTER DESIGN

The basic principle involved in a frequency counter is shown in Figure 1. The counter consists of an accurate time base, a sampling gate, and a counter chain. To measure the incoming frequency, the time base opens the sampling gate to the counter chain for a known period of time and then closes the gate again. The counter chain stores the number of pulses coming in during the sample time period that the gate is open. Using this number in association with the amount of time the gate was open will provide an accurate measurement of the frequency.

The maximum frequency that can be recorded and displayed (assuming the counter can operate fast enough) is determined by the number of stages in the counter chain and the length of time the input is gated on. The maximum frequency is:

$$f_{max} = \frac{10^N - 1 \text{ pulses/sample period}}{Tp \text{ seconds/sample period}}$$

where f_{max} = maximum frequency in hertz
N = number of ÷ 10 stages in counter
Tp = sample period

To use the example of the MECL – McMOS design, a seven stage ÷ 10 counter chain can hold a maximum number of 9,999,999. If the sample period is one second, the maximum frequency that can be recorded is $10^N - 1$ Hz or any frequency less than 10 MHz. A graphic display of the maximum frequency with various time bases is shown in Figure 2.

It can be observed that accuracy is determined by the length of the sampling period and the number of stages in the counter chain. If a long sample period is used with a large N-stage counter, extremely good accuracy can be obtained, even for very high frequencies. However, in any

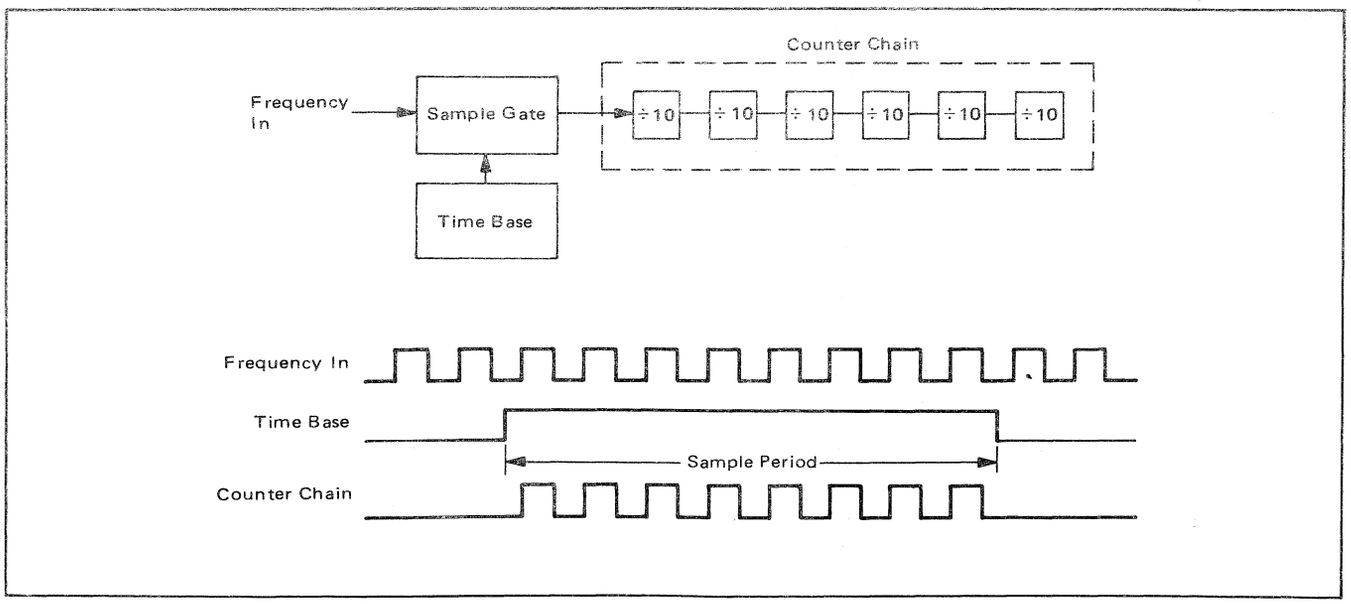

FIGURE 1 – Block Diagram and Timing Diagram of Frequency Counter

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frequency counter design there is a practical limit on the number of stages in the counter and the maximum length sample period.

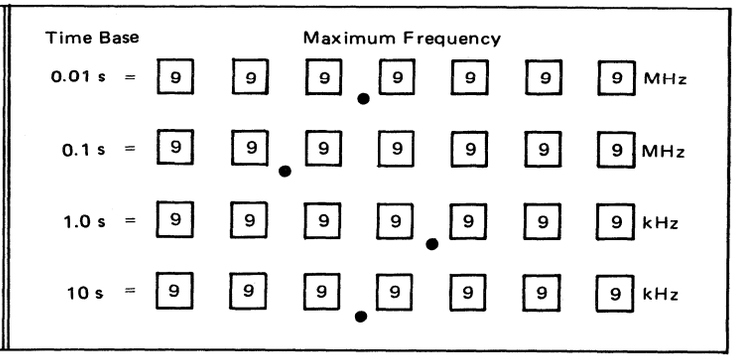
With any frequency counter it is best to select a time base which will display the maximum number of significant digits for a given frequency. That is, the longest sample period that can be used for a given frequency should be selected to display the maximum number of significant figures for best accuracy.

Also, the time base must be altered according to the prescaler to maintain the proper frequency reading within the counter chain. This will be demonstrated in the MECL – McMOS counter.

MECL – McMOS DESIGN

The block diagram of the autoranging counter is shown in Figure 4. The design consists of a 7-stage counter chain and display, autorange logic, time base and control logic, sample gate and ÷2 prescaler. The system requires +5 volt and -5 volt power supplies. The McMOS devices operate at 10 volts differential (V_{DD} = +5 volts, V_{SS} = -5 volts) and the MECL 10,000 devices use -5 volts (V_{CC} = ground, V_{EE} = -5 volts).

FIGURE 2 – Maximum Frequencies That Can Be Measured with a 7-Stage Counter for Various Time Base



Autoranging is the ability of a test instrument to do this function automatically. Normally, the person using the instrument selects the time base manually; however, with autoranging, the instrument monitors the incoming frequency readings and adjusts itself accordingly. The only disadvantage to this scheme is that a couple of sampling periods may be required for the counter to adjust itself to the proper time base.

One other technique used in counter design should be noted before advancing to the MECL – McMOS counter. This technique is called prescaling as shown in Figure 3. The basic counter configuration of Figure 1 is altered by the addition of a ÷M stage prior to the sampling gate. Normally M is equal to 2 or 10 for ease of use and display.

The operation is similar to the basic counter configuration of Figure 1. The autorange logic monitors the contents of the counter chain, and in association with the control logic selects the proper time base. The use of prescaling extends the frequency range of the counter to over 200 MHz. Additional features of frequency check and manual time base selection are also included.

Each section of the design will be explained in more detail.

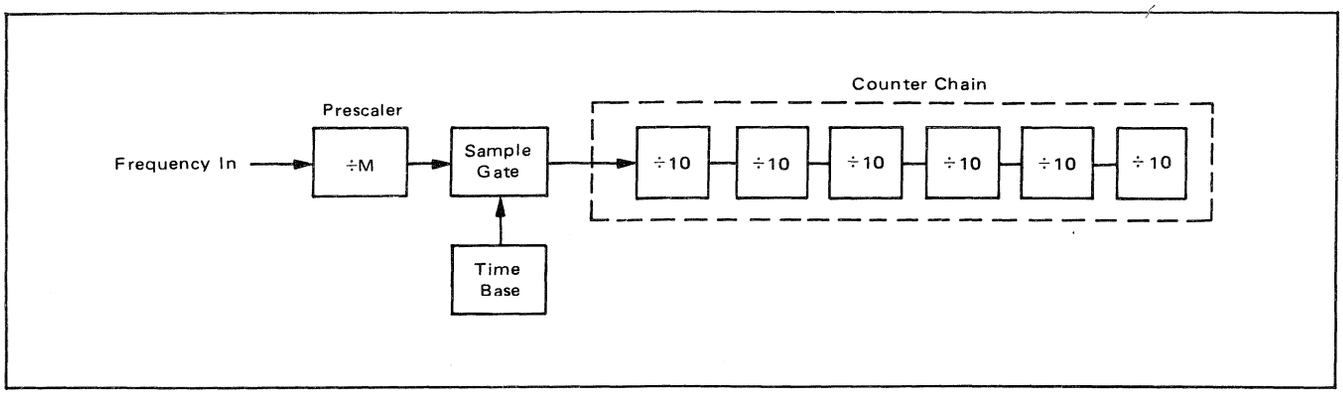


FIGURE 3 – Block Diagram of Frequency Counter with Prescaler

In effect, the usable range of the frequency counter has been extended because the prescaler will work at a much higher frequency than the counter chain. The disadvantage is that some accuracy is lost by the counter because the prescaler is not turned on and off by the sampling gate, and the exact count is not defined within the extent of the prescaler modulus M.

COUNTER CHAIN AND DISPLAY

The basic counter chain consists of 7 decade stages with a 6 digit display. The first 2 stages are MECL 10,000 MC10138 decade counters used in a ripple mode. The remaining 5 stages are the McMOS MC14518 dual BCD counters in fully synchronous operation. The counter chain and display are shown in the diagram of Figure 5.

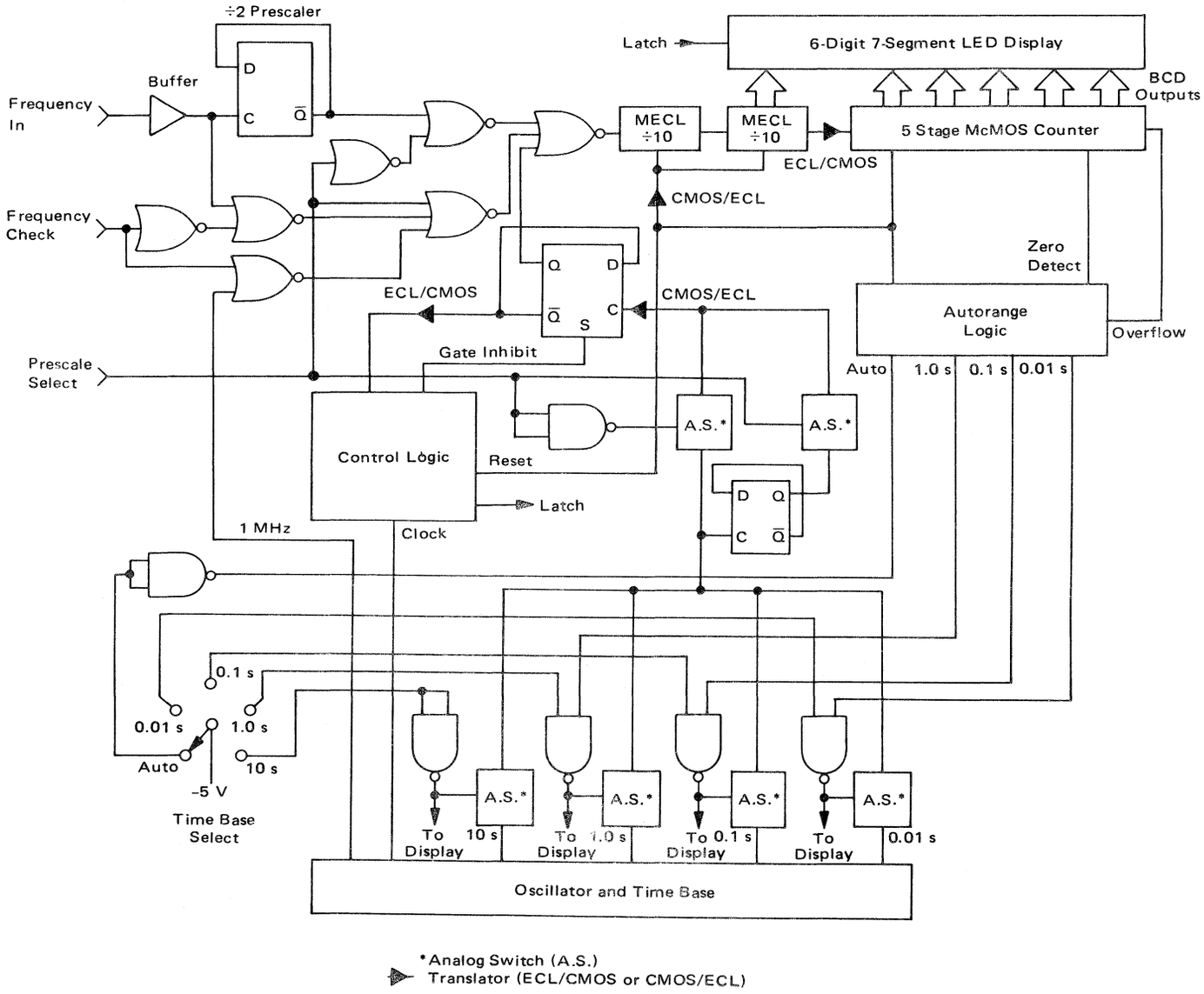


FIGURE 4 – Block Diagram of 200 MHz Autoranging Counter

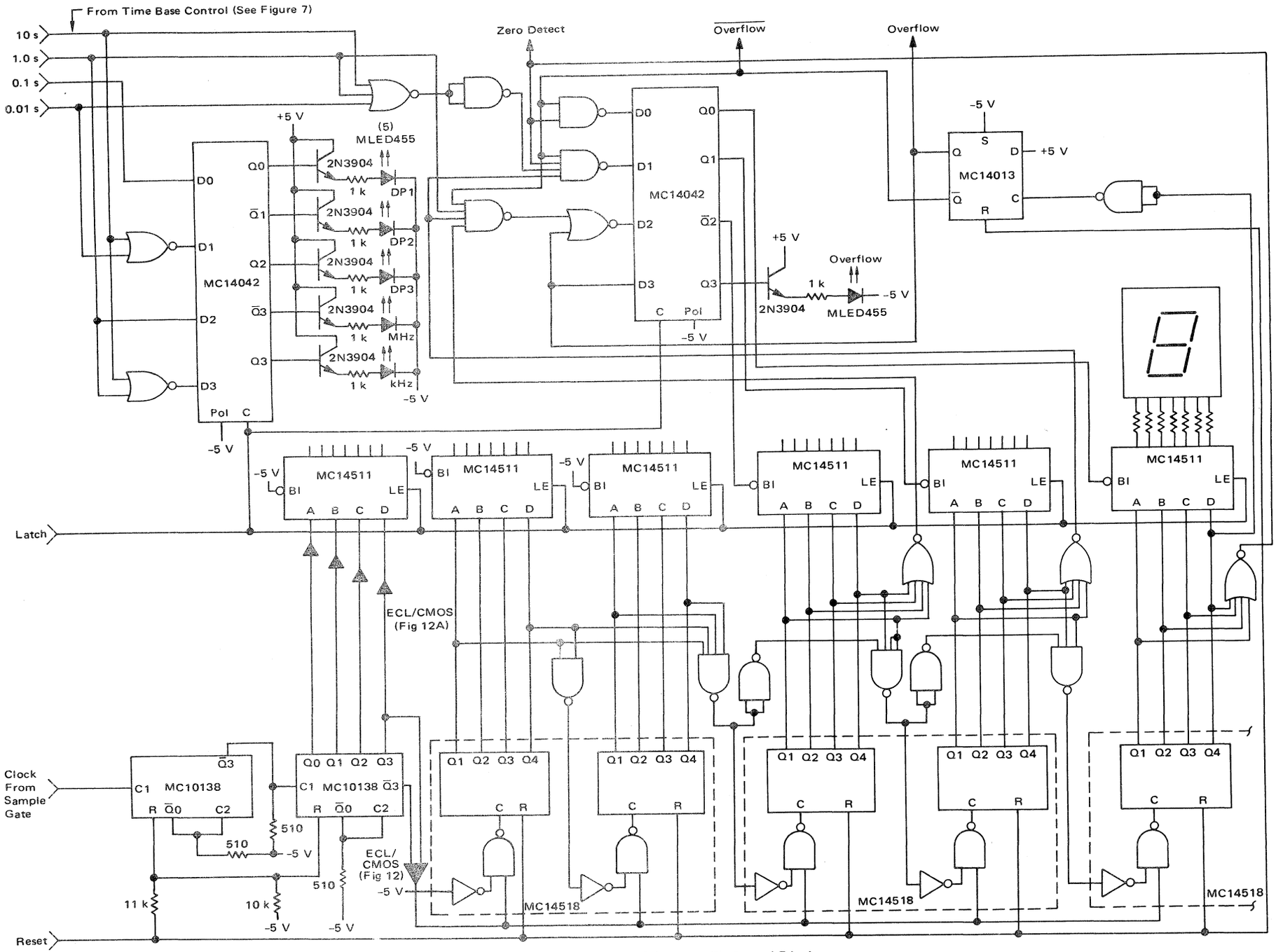


FIGURE 5A – Schematic Diagram of Counter Chain and Display

The maximum frequency of operation of the counter chain is approximately 120 MHz, limited by the McMOS synchronous counter. With the MECL 10,000 devices used in a ripple mode, the maximum frequency into the McMOS counter is then 1.2 MHz. Notice that translators are necessary to drive the McMOS clock line and the display inputs from the MECL counter. The translators will be discussed in more detail later.

The display shows the 6 most significant digits, although the least significant digit could be shown if the designer chooses. The BCD outputs of the counters are strobed into the MC14511 latch/decoder/drivers. Utilizing the zero blanking capability of the MC14511, the display has leading zero suppression.

In additional to zero suppression, logic is shown for the generation of the proper decimal point location and frequency scaler (kilohertz or megahertz). The counter uses 0.01 s, 0.1 s, 1.0 s, and 10 s time bases. With the display composed as in Figure 5B, the frequency would be shown similar to Figure 2.

Note that overflow is also latched and shown on the display.

AUTORANGE LOGIC

The autorange logic monitors the state of the counter chain and adjusts the time base to display the greatest number of significant digits. The time bases used in the autorange mode are 0.01 s, 0.1 s, and 1.0 s. The 10 s base is not used because the sampling rate is too slow for convenient use. This means that for any frequency below 10 MHz the time base will remain 1.0 s. If the frequency is 10 MHz or higher, the time base will become 0.1 s. In turn, a 0.1 s sample period is sufficient for any frequency less than 100 MHz. At 100 MHz and above, the sample period becomes 0.01 s.

Referring to Figure 6, inputs are taken from the most significant digit (zero detect) and counter overflow to determine the proper time base. Also, the existing time base is monitored to allow the time base to move up or down as required by the input frequency.

If the counter is on the 1.0 s base and overflow occurs, the counter jumps to the 0.1 s base. The sample period will remain at 0.1 s unless overflow again occurs or the most significant digit is zero with no overflow. Either condition will change the time base – to 0.01 s with over-

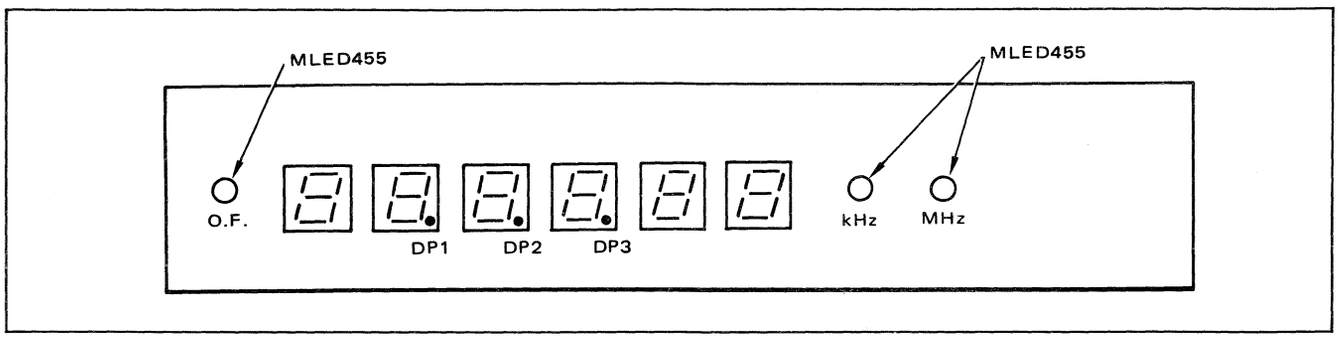


FIGURE 5B – Physical Arrangement of Counter Display

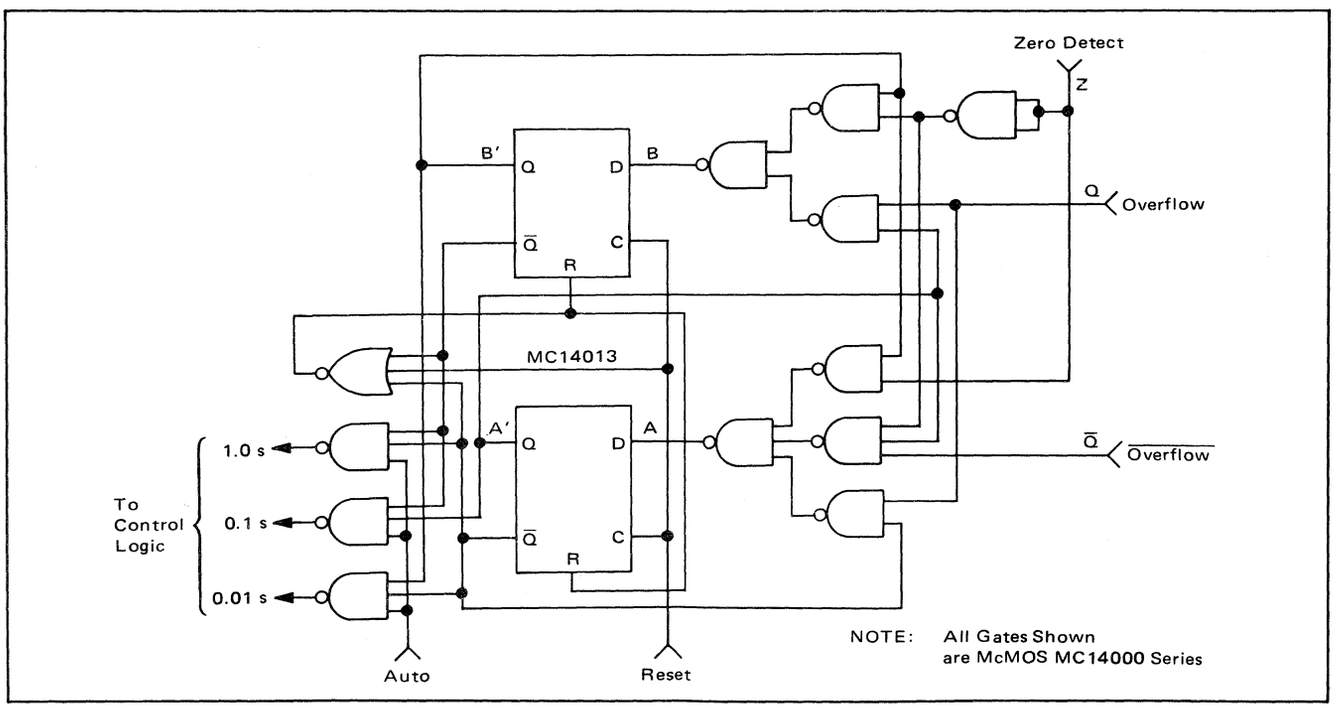


FIGURE 6 – Autorange Logic Schematic Diagram

flow or to 1.0 s with zero detect and no overflow. In the 0.01 s time base no overflow can occur as the toggle capability of the counter is not great enough. Therefore, the time base will return to 0.1 s if zero detect occurs.

The possible conditions are:

	A′	B′	Z	Q	A	B
1.0 s	0	0	X	0	0	0
	0	0	X	1	1	0
0.1 s	1	0	0	0	1	0
	1	0	X	1	0	1
	1	0	1	0	0	0
0.01 s	0	1	0	0	0	1
	0	1	1	X	1	0

X = Don't Care

The logic equations for inputs A and B to the flip-flops are:

$$A = \overline{(A' \, Q \, \bar{Z}) \cdot (\bar{A}' \, Q)} \cdot \overline{(B' \, Z)}$$

$$B = \overline{(B' \, \bar{Z}) \cdot (A' \, Q)}$$

The flip-flops are updated by the leading edge of the reset pulse. The flops act as a holding register, so the counter can be reset and then allowed to take a new sample reading.

The flip-flop outputs are decoded to provide the proper time base:

A	B	Time Base
0	0	1.0 s
1	0	0.1 s
0	1	0.01 s
1	1	Not used

If the unused state occurs due to noise or start up, the flip-flops are set to the 1.0 s time base.

The autorange logic is always functioning; however, manual operation may be desired. The Time Base Select switch will disable the autorange outputs and cause the selected time base to be used.

TIME BASE AND CONTROL LOGIC

The time base and control logic maintain the actual operation of the counter. Observing Figure 7 it can be seen that the various sample periods are generated from a 1 MHz crystal oscillator and several ÷10 counters. Seven counters are necessary to produce the longest period of 10 s from a 1 MHz source (1.0 μs).

The MC12060 is used in the design for the crystal oscillator. The MC12060 consists of the basic oscillator circuit with ECL and TTL translators. In Figure 7, the ECL translator is used to drive an ECL/CMOS translator to the clock of the first McMOS ÷ 10 counter. Also, the ECL output provides a 1 MHz signal for the frequency check. A separate section will describe the translator used here and other translators used in the design.

The different time bases are selected by the Time Base Select switch. The switch will select a specific time base or activate the autorange logic to provide the appropriate time base. Analog switches are used to steer the selected time base to the clock input of the Gate Flip-Flop.

It can be noted also, that the Prescaler input will cause the selected sample period to be doubled in value. That is, if the sample period has a rate of one pulse per second, the Prescaler input will cause the signal to be divided by 2, and the signal into the Gate Flip-Flop will have a rate of one pulse every two seconds. The reason for the time base modification is that the prescaler divides the frequency entering into the counter by a factor of 2. Therefore, the sample period must be twice as long to provide the proper frequency reading on the counter.

The time base signal is free-running with respect to the Gate Flip-Flop. However, the latch, reset, and gate inhibit signals used in conjunction with the Gate Flip-Flop are synchronously generated by the control logic.

Consider the timing diagram of Figure 8. The Q output of the Gate Flip-Flop is low when the frequency counter is taking a reading. The rising edge of the time base signal clocks the Gate Flip-Flop, and in turn, this fires the MC14528 one-shot (the Q output of the MC14528 goes high). As soon as the one-shot fires, the first positive transition of the control logic clock (0.1 MHz signal from the time base logic) will change the state of the shift counter formed by the MC14027 J-K flip-flops.

The shift counter will produce the decoded latch and gate inhibit signals. The latch signal goes low for one clock period to update the reading on the counter display. The gate inhibit signal goes high to prevent the Gate Flip-Flop from toggling again.

The latch and gate inhibit outputs will remain in this condition until the MC14528 times out and returns to its normal state. In this manner, the one-shot controls the sample rate at which the counter operates. With the values of R and C shown, the sample rate can be varied from about 1.0 to 4.5 seconds.

When the one-shot returns to its normal state (Q output low), a reset pulse of one clock period is generated. The reset pulse returns the counter chain to zero, restores the overflow flip-flop to its normal state, and updates the autorange logic. At the end of the reset pulse, the gate inhibit also goes low.

The counter will then be ready to take a new measurement of the incoming frequency. The new sample period will begin on the next positive transition of the time base signal to the Gate Flip-Flop. The entire cycle will be repeated at the end of the new sample period.

PRESCALER AND SAMPLE GATE

The prescaler and sample gate logic of Figure 9 selects one of three sources for the frequency into the counter chain. The Operation Select switch will allow normal operation, prescale, or frequency check.

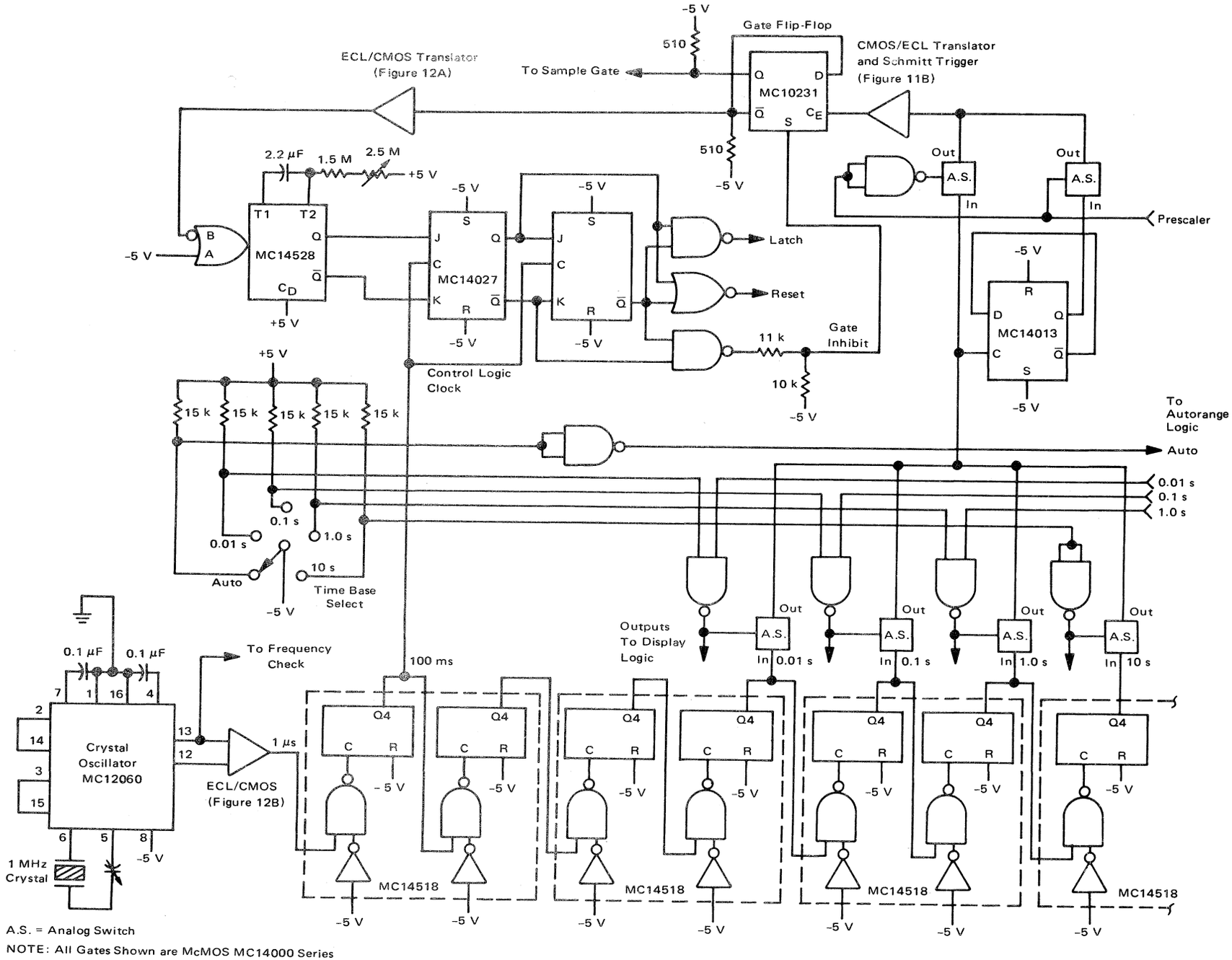


FIGURE 7 – Control Logic and Time Base Schematic Diagram

In normal operation the incoming signal is "conditioned" by the input buffer and routed directly to the sample gate. The maximum frequency in this mode is about 125 MHz because of the bandwidth limitation of the MECL 10,000 gate and the counter chain.

For higher frequencies, prescale operation is used, and the signal is divided by 2 by the MC10231 flip-flop. The worst case toggle frequency is guaranteed as 200 MHz minimum at 25°C for this flip-flop. The counter will then have a toggle capability of 200 MHz minimum and 225 MHz typical. Also, prescale selection will cause the proper time base modification (Figure 9).

The frequency source is the frequency check. A 1 MHz signal is obtained from the oscillator and provides an accurate test frequency.

An MC10109 is used as the sample gate. A signal from the Gate Flip-Flop opens the sample gate for the amount of time determined by the selected time base to make frequency measurements.

The buffer used in the logic of Figure 9 can vary depending on the application of the counter. The buffer should be a 200 MHz wide-band amplifier with high input impedance or 50-ohm compatible input impedance. Also, multiple buffers could be used – one amplifier for low frequencies and another for high frequencies.

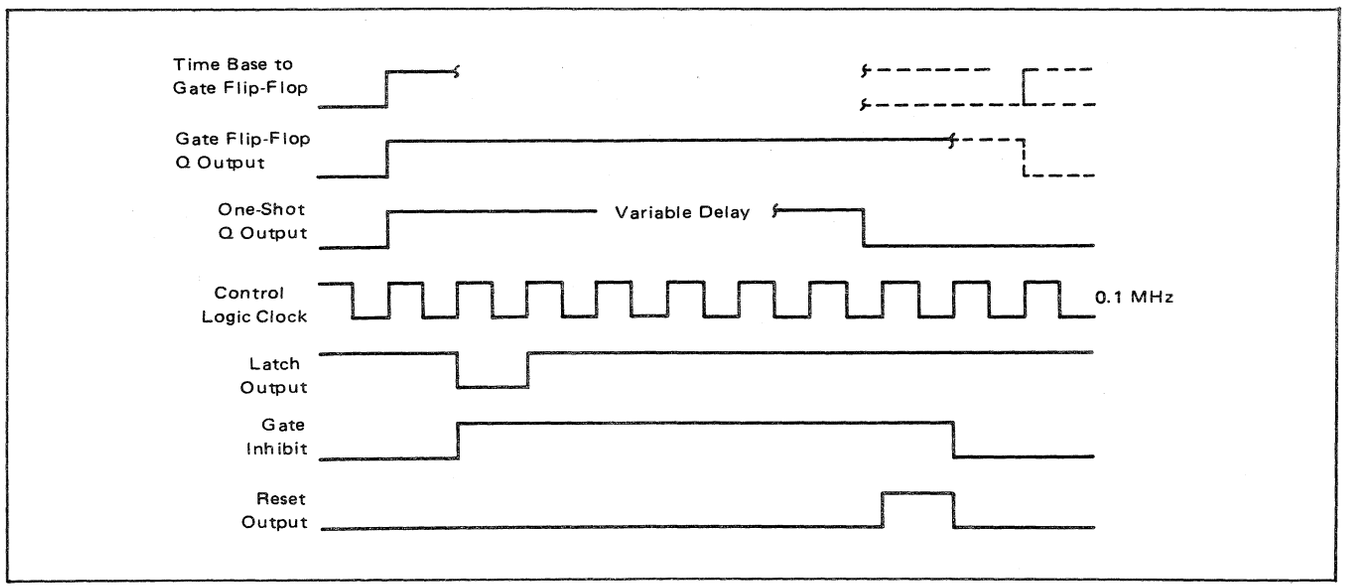


FIGURE 8 – Control Logic Timing Diagram

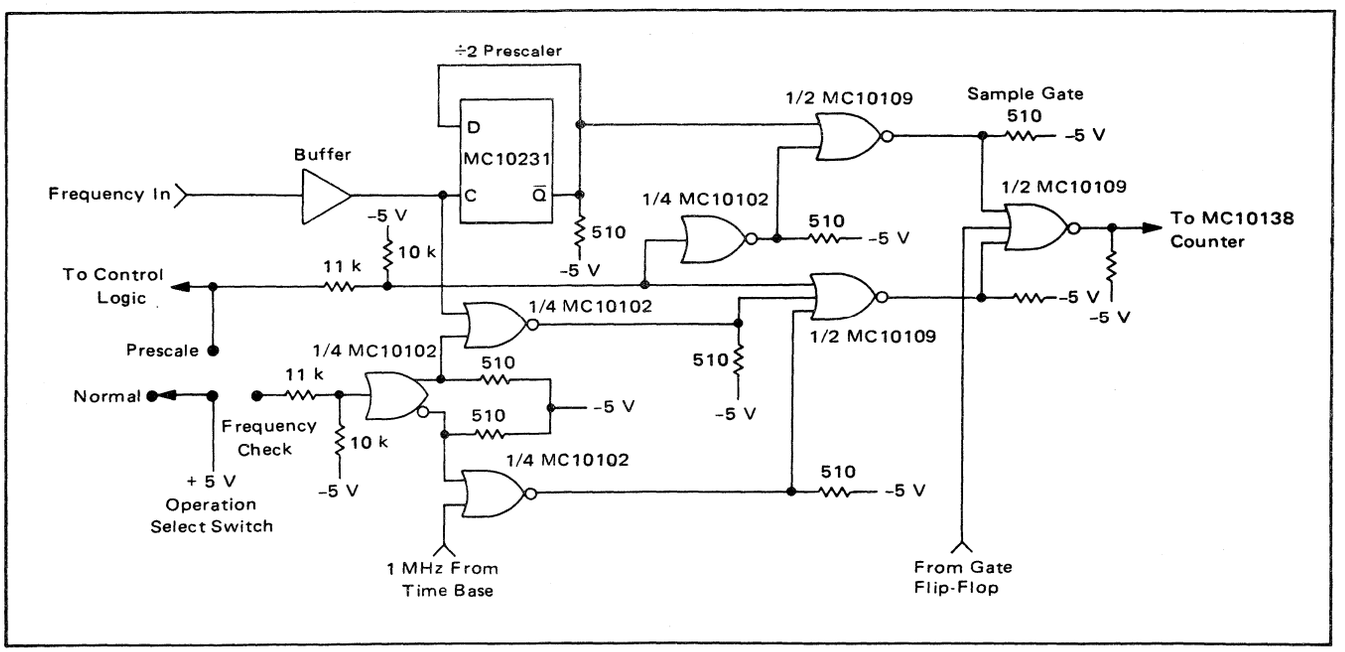


FIGURE 9 – Prescaler and Sample Gate Logic

An example of a 200 MHz wide-band amplifier with high input impedance is shown in Figure 10. The design is an adaptation of an amplifier from Motorola application note AN-581. The output is MECL 10,000 compatible, and Schmitt trigger action is incorporated. The input impedance could also be made 50 ohms to ground for coaxial cable termination. Sensitivity is about 50 mV peak-to-peak.

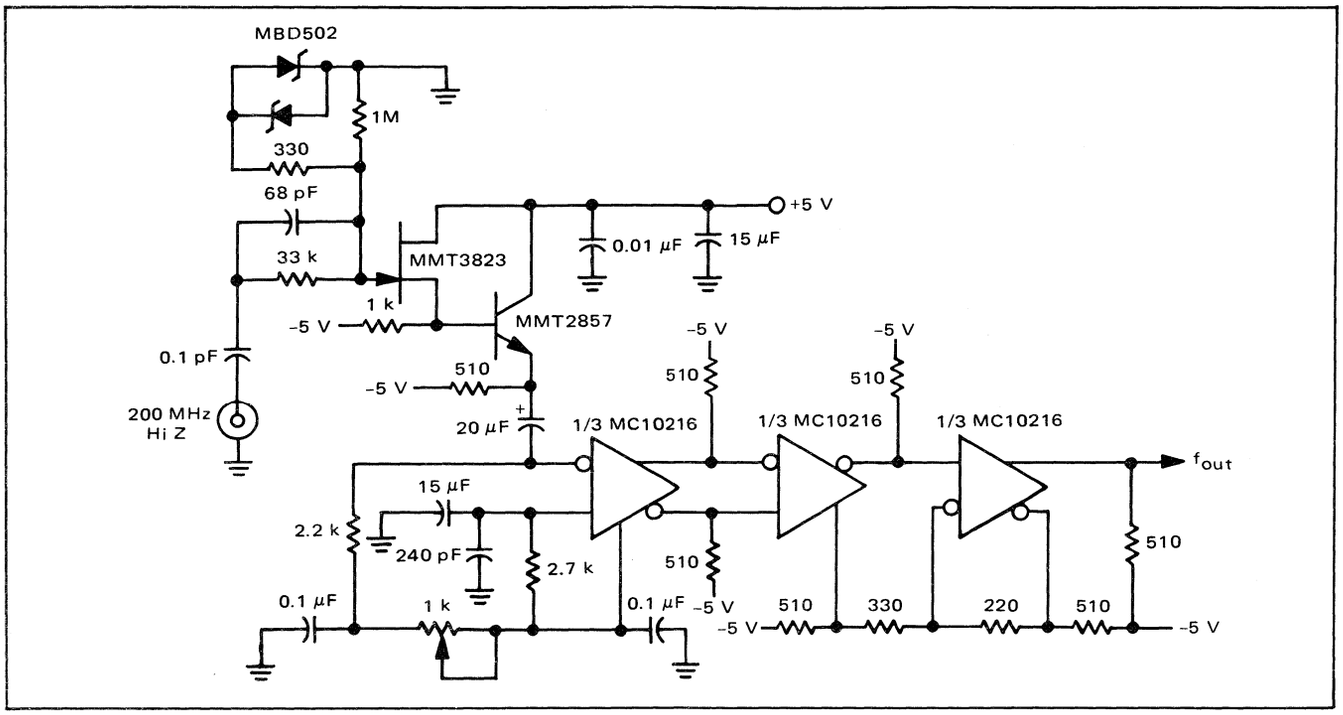


FIGURE 10 – 200 MHz Buffer Amplifier

TRANSLATORS

The use of two logic forms requires translation between logic voltage levels. The McMOS is operated with a voltage potential of 10 volts to obtain the required operating speed, and the MECL 10,000 requires a -5 volt supply. Thus, the power supply voltages are +5 volts and -5 volts. The plus and minus voltages are also useful for designing an input buffer amplifier that can be biased at ground potential for dc coupling.

Translators are required both going from CMOS to ECL and ECL to CMOS. The easier case is translating from CMOS to ECL. The CMOS swings the full voltage from +5 volts to -5 volts. A resistor attenuation network can be used to convert to ECL compatible levels. MECL 10,000 levels are approximately -0.9 volt logic high and -1.7 volts logic low. The high level should not get more positive than ground; however, the low level can go as low as the negative supply. The resistor array of Figure 11A attenuates the +5 volt to -5 volt output swing of CMOS to approximately -0.4 volt in the high state and -5 volts in the low state for ECL.

In the MECL – McMOS counter all ECL/CMOS translators are as shown in Figure 11A except for the translator at the clock input of the Gate Flip-Flop. The relatively slow edge speeds of CMOS can result in noise on the clock input of an ECL flip-flop. Therefore, a Schmitt trigger is added to the translator (Figure 11B) to eliminate any such problems.

The conversion of ECL levels to CMOS requires active devices to boost the 0.8 volt swing of ECL to the 10 volt swing of CMOS. The more simple translator is a two transistor switch as illustrated in Figure 12A. The circuit has a passive resistor pullup on the collector of the NPN

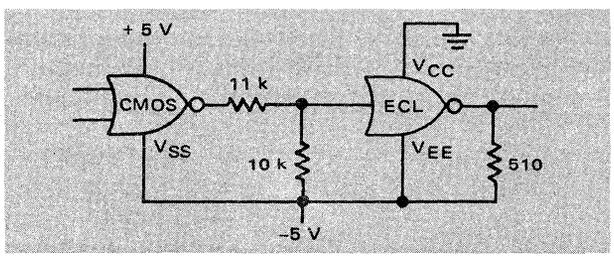


FIGURE 11A – CMOS/ECL Translator

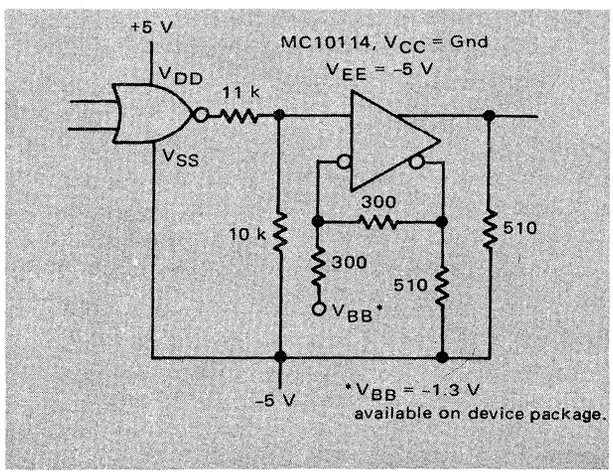


FIGURE 11B – CMOS/ECL Translator with Schmitt Trigger

transistor, and the translator is used for the counter display and on the Q output of the Gate Flip-Flop.

A faster version is shown in Figure 12B. An active pullup is added to the output of the translator to get faster rise times. A faster circuit is required for driving the McMOS synchronous counter from the MC10138 and for driving the 1 MHz clock input to the McMOS time base counter. Note that the Q3 output of the MC10138 must go to the base of the PNP transistor of the translator (Figure 5A).

Complementary ECL outputs are used to drive the faster translator. The PNP transistor of Figure 12B can be driven in a manner similar to Figure 12A if the designer so desires. Use of the complementary outputs, however, eliminates the need for a silicon diode at the emitter of the PNP device.

CONCLUSION

Many variations of the MECL – McMOS counter could be made. A more sophisticated time base could be employed, a different display such as liquid crystal could be used, or different input buffers could be designed. The desired application of the counter will determine such changes. Also, the discussion of the counter does not include detailed information on building the instrument. The designer seeking more information on wiring rules and usage rules is directed to the Motorola McMOS Handbook and the MECL System Design Handbook.

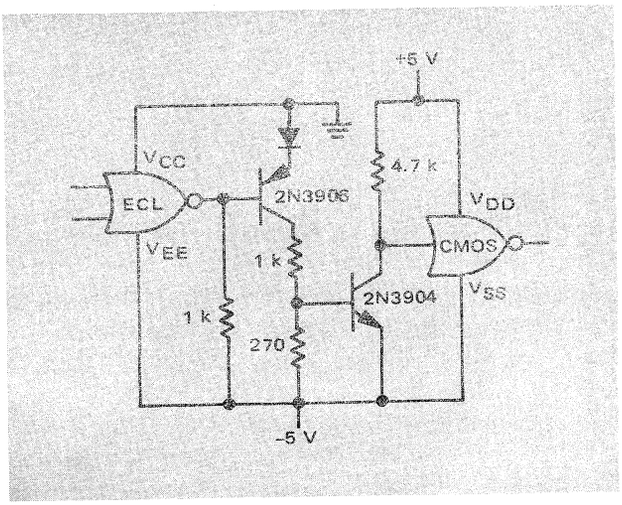


FIGURE 12A – ECL/CMOS Translator with Passive Pullup

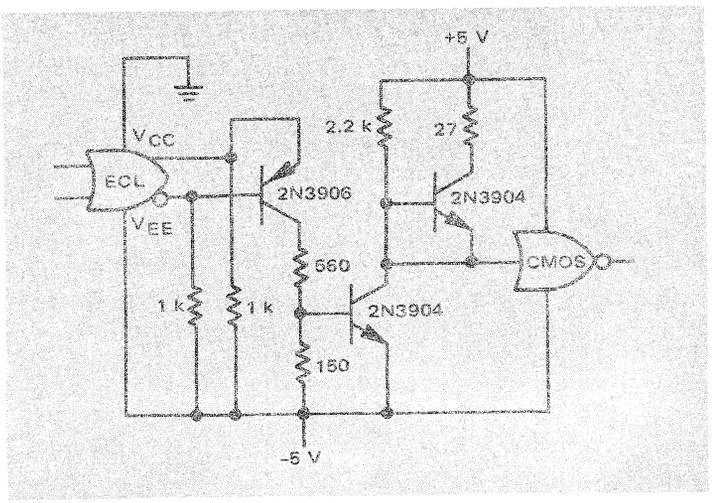


FIGURE 12 B – ECL/CMOS Translator with Active Pullup

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